AMENDMENTS TO THE CLAIMS

This listing of claims replaces all prior versions, and listings, of claims in the application:

Listing of Claims:

1. **(Currently Amended)** A matrix converter comprising:

an input terminal;

an output terminal; and

current commutation circuitry having a matrix switch arrangement including a plurality of power semiconductor bi-directional switches arranged in a matrix configuration, each said switch directly connected between the input terminal and the output terminal of the converter, said matrix switch arrangement performing ~~timing/delay~~ timing operations effecting commutation functions with initiation of one switch before de-activation of another switch wherein the matrix switch arrangement provides a commutation interval which approaches or equals zero.

2. **(Currently Amended)** A converter according to Claim 1 wherein the matrix switch arrangement comprises a first switch and a second switch whereby, in a first mode in use, the first switch is activated and the second switch is not activated, and the matrix switch arrangement performs ~~timing/delay~~ timing operations which activates the second switch before the first switch is de-activated.

3. **(Currently Amended)** A converter according to Claim 1 wherein the matrix switch arrangement comprises circuitry performing ~~timing/delay~~ timing operations of the switches to minimize the commutation interval.

4. **(Currently Amended)** A converter according to Claim 1 wherein the matrix switch arrangement comprises circuitry performing ~~timing/delay~~ timing operations of the switches to provide a commutation interval of less than those typically used as a deadtime in a Voltage Source Inverter.

5. **(Cancelled)**

6. **(Currently Amended)** A converter according to Claim 1 wherein the matrix switch arrangement comprises circuitry performing ~~timing/delay~~ timing operations of the switches to provide a commutation interval which is negative.

7. **(Cancelled)**

8. **(Previously Presented)** A converter according to Claim 1 wherein the converter comprises the plurality of bi-directional switches configured to effect reduction of the commutation interval.

9. **(Cancelled)**

10. **(Currently Amended)** A method of operating a matrix converter having a matrix switch arrangement including a plurality of power semi-conductor bi-directional switches arranged in a matrix configuration and directly connected between an input terminal and an output terminal, the method comprising operating said matrix switch arrangement to perform ~~timing/delay~~ timing operations effecting commutation functions with activation of a first switch before de-activation of a second switch wherein a commutation interval approaches or equals zero.

11. **(Previously Presented)** A method according to claim 10 wherein, in a first mode, in use, the first switch is activated and the second switch is not activated and then the matrix switch arrangement activates the second switch before the first switch is de-activated.

12. **(Currently Amended)** A method according to claim 10 wherein the matrix switch arrangement ~~performs/delay~~ performs timing operations on the switch thereby minimizing the commutation interval.

13. **(Currently Amended)** A method according to claim 10 wherein the matrix switch arrangement performs ~~timing/delay~~ timing operations on the switch thereby providing a commutation interval of less than those typically used as a deadtime in a Voltage Source Inverter.

14. **(Cancelled)**

15. **(Currently Amended)** A method according to claim 10 wherein the matrix switch arrangement performs ~~timing/delay~~ timing operations on the switch thereby providing a commutation interval which is negative.

16. **(Cancelled)**

17. **(Currently Amended)** A method according to claim 10 wherein the matrix switch arrangement performs ~~timing/delay~~ timing operations on the switch thereby to effect reduction of the commutation interval.

18.-22. **(Cancelled)**

23. **(Currently Amended)** A converter according to Claim 1 wherein the matrix switch arrangement comprises ~~timer/delay~~ timing operations of the power semiconductor bi-directional switches by at least one of:

setting timer switches to set at least one timer to implement a delay and to set a clock speed to the at least one timer to control at least one of a reverse switch of time, a commutation time, and a reverse switch on time.

~~according to any one or more of Tables 6 to 11.~~

24. **(Currently Amended)** A method according to Claim 10 comprising the matrix switch arrangement performing ~~timing/delay~~ timing operations of the power semiconductor bi-directional switches by at least one of:

setting timer switches to set at least one timer to implement a delay and to set a clock speed to the at least one timer to control at least one of a reverse switch of time, a commutation time, and a reverse switch on time.

~~according to one or more of Tables 6 to 11.~~

25. **(New)** The converter of claim 1, wherein the timing operations comprise delays including at least one of: a reverse switch of time; a commutation time; and a reverse switch on time.

26. **(New)** The converter of claim 10, wherein operating said matrix switch arrangement to perform timing operations further comprises setting delays including at least one of: a reverse switch of time; a commutation time; and a reverse switch on time.

27. **(New)** The matrix converter of claim 25, wherein the timing operations are set to achieve a particular output waveform.

28. **(New)** The matrix converter of claim 27, wherein the timing operations are determined by at least one timer, wherein the at least one timer is set to produce at least one of the reverse switch off time, the commutation time, and the reverse switch on time in the plurality of power semiconductor bi-directional switches.